

Claims:

1. A circuit board, comprising:
 - a first laminate made of a fusible dielectric material;
 - 5 a second laminate made of a fusible dielectric material bonded to the first laminate along respective inner faces thereof;
 - a plurality of exposed first electrical contacts on an outer face of the first laminate;
 - a plurality of exposed second electrical contacts on an outer face of the second
 - 10 laminate; and
 - a plurality of electrical conductors each running from a first contact to a second contact, the conductors including elongated conductive lines extending along one of the first or second laminates and vias extending through the first and second laminates which have been filled with an electrically conductive filler.
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2. The circuit board of claim 1, wherein each of the laminates comprises reinforcing fibers having impregnated by a resin.
3. The circuit board of claim 2, wherein the first electrical contacts are configured
- 20 as die pads and the second electrical contacts are configured as solder ball bond pads, whereby the circuit board can be used as a flip-chip integrated circuit package substrate.
4. The circuit board of claim 3, wherein the via filler consists essentially of an adhesive containing conductive metal particles, and the conductive lines consist
- 25 essentially of a plated metal disposed between an outer surface of at least one of the first and second laminates and an external soldermask layer.
5. The circuit board of claim 4, wherein the via filler consists essentially of a transient liquid phase sintering conductive adhesive wherein the metal particles have
- 30 been sintered after filling of the adhesive into the via.
6. The circuit board of claim 1, wherein the first and second laminates are directly bonded to each other, and at least one of a ground plane and a power plane is embedded between the first and second laminates.

7. The circuit board of claim 5, wherein the first and second laminates are directly bonded to each other, and at least one of electrical conductors suitable for use as an integrated circuit power supply and suitable for use as an integrated circuit electrical ground connection is embedded between the first and second laminates.

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8. The circuit board of claim 1, further comprising a third laminate made of a fusible dielectric material, which third laminate is interposed between and bonded to each of the first and second laminates, and electrical conductors suitable for use as an integrated circuit power supply and integrated circuit electrical ground connection are embedded between laminates on opposite sides of the third laminate.

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9. The circuit board of claim 1, wherein the first and second laminates are free of layer to layer contact with a metallic support plate.

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10. A process for making a circuit board, comprising:

forming a first subassembly, wherein the first subassembly includes a first rigid support plate, a first laminate made of a fusible dielectric material bonded to the rigid support, and a first circuit pattern including a number of vias through the first laminate filled with an electrically conductive filler;

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forming a second subassembly, wherein the second subassembly includes a second rigid support plate, a second laminate made of a fusible dielectric material bonded to the rigid support, and a second circuit pattern including a number of vias through the second laminate filled with an electrically conductive filler, wherein vias in an inner surface of the first laminate can be brought into electrical contact with the circuit pattern of the second laminate, and vias in an inner surface of the second laminate can be brought into electrical contact with the circuit pattern of the first laminate;

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bonding the inner surfaces of the first and second laminates together to form electrical connections at the aligned filled vias; and

removing the rigid supports from outer faces of the first and second laminates.

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11. The process of claim 10, wherein the step of forming the first subassembly comprises:

forming a first release layer on a face of the first rigid support;

forming a first electrically conductive metal layer on the release layer;

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placing a first laminate made of a dielectric material comprising fibers having a resin impregnated therein over the first release layer and first conductive layer;

forming vias through the first laminate at locations overlying the electrically conductive metal layer; and

filling the vias in the first laminate with an electrically conductive filler material.

- 5 12. The process of claim 11, wherein the step of forming the second subassembly comprises:

forming a second release layer on a face of the second rigid support;

forming a second electrically conductive metal layer on the second release layer;

- 10 placing a second laminate made of a dielectric material comprising fibers having a resin impregnated therein over the second release layer and second conductive layer;

forming vias through the second laminate at locations overlying the electrically conductive metal layer; and

filling the vias in the second laminate with an electrically conductive filler material.

- 15 13. The process of claim 12, wherein the step of removing the rigid supports comprises removing the first rigid support from the first release layer and removing the second rigid support from the second release layer.

- 20 14. The process of claim 13, further comprising, follow the step of removing the rigid supports, a step of removing the release layers.

- 25 15. The process of claim 14, wherein the rigid supports each comprise a steel plate and the release layers each comprise a thin copper layer, and the step of removing the release layers comprises chemically etching the thin copper layers.

- 30 16. The process of claim 15, wherein the electrically conductive metal layers each comprise a sublayer of copper and a sublayer of a metal resistant to an etchant used to etch the thin copper layers, wherein the etchant-resistant metal is interposed between the copper sublayer and the thin copper release layer.

- 35 17. The process of claim 10, further comprising:
forming a third circuit pattern on at least one of the first and second laminates;
and

during the bonding step, embedding the third circuit pattern between the first and second laminates.

18. The process of claim 17, wherein the third circuit pattern comprises at least one of:

an electrical conductor suitable for use as an integrated circuit power supply, and
an electrical conductor suitable for use as an integrated circuit electrical ground
5 connection.

19. A flip-chip integrated circuit package substrate, comprising:
a first laminate made of a fusible dielectric material;
a second laminate made of a fusible dielectric material bonded to the first
10 laminate along respective inner faces thereof;
a plurality of exposed die pads on an outer face of the first laminate;
a plurality of exposed solder ball bond pads on an outer face of the second
laminate;

a plurality of electrical conductors each running from a die pad contact to a solder
15 ball bond pad, the conductors including elongated conductive lines extending along one
of the first or second laminates and vias extending through the first and second laminates
which have been filled with an electrically conductive filler; and

a heat sink having a central opening therein bonded to the outer face of the first
laminate, wherein the die pads are accessible through the central opening in the heat sink.
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20. The flip-chip integrated circuit package substrate of claim 19, wherein each
of the laminates comprises reinforcing fibers having impregnated by a resin.

21. A flip-chip integrated circuit package, comprising:
25 a substrate including a plurality of exposed die pads on a die side of the substrate,
a plurality of exposed solder ball bond pads on a ball side of the substrate, and a plurality
of electrical conductors each running from a die pad to a solder ball bond pad, the
conductors including elongated conductive lines extending along the substrate and
interconnects extending through the substrate;

30 a heat sink having a central opening therein bonded to the die side of the
substrate, wherein the die pads are accessible through the central opening in the heat sink;
an integrated circuit die positioned in the central opening of the heat sink in
contact with the die pads; and

a layer of an encapsulant surrounding the die, wherein the layer of an encapsulant
35 contains a heat conducting material that conducts heat from the die to the heat sink better
than the encapsulant by itself.

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22. The flip-chip integrated circuit package of claim 21, wherein the heat conducting material comprises metal particles distributed in the encapsulant between the die and the heat sink.

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23. The flip-chip integrated circuit package of claim 21, wherein the encapsulant comprises a curable resin.

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FOR REVIEW